

REMARKS

In response to the above-identified Office Action, Applicant amends the application and seeks reconsideration thereof. Applicant amends claims 1-2, 4-5, 8 and 10. Applicant cancels claim 3. Applicant respectfully requests reconsideration of claims 1-2 and 4-10, as amended, in view of at least the following.

I. Claims Rejected Under 35 U.S.C. §102

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,326,702 to Lee, et al. ("Lee"). It is axiomatic that to anticipate every limitation of a claim must be disclosed in a single reference.

Applicant respectfully disagrees with the rejection above and submits that independent claim 1 is patentable over the cited references for at least the reason that the cited reference does not disclose a dielectric layer having a first thickness over a gate and a different second thickness over a junction region, and forming a contact opening through the dielectric layer to the gate comprising etching for a period of time between a time necessary to etch through the dielectric layer on the gate region and a time necessary to etch through the dielectric layer and to the junction region, as required by amended claim 1. According to claim 1, for example, a contact opening may be formed through a dielectric layer that is thinner over the gate than the junction region adjacent to the gate by etching for a period of time sufficient to allow the opening to reach the gate, but for less than a period of time sufficient to allow the opening to extend deeper through the dielectric adjacent to the gate and to the junction region (see **Figures 3-4 and 12-13** of the application as originally filed). Similarly, the contact opening may

extend into the dielectric adjacent to the gate, to a lesser depth down the first thickness (e.g., see **Figures 6 and 9**).

Lee teaches using silicon nitride layer 119 as an etch stop layer during sequentially etching layers 130 and 120 to define contact tolls 131a through 131e (See col. 9, lines 35-51 and Figure 5). In particular, Lee teaches using the thickness of layer 119 and multiple etches using different etchants to control etching to expose regions 105, 115 and 117 (see col. 9, lines 51 through col. 10, line 3).

However, Lee does not teach the above-noted limitations of claim 1. Specifically, layer 119 is a blanket layer and therefore does not have a first thickness over the gate and a second different thickness over the junction region (see col. 9, lines 42-43). Moreover, Lee does not teach etching layer 130 or 120 where a period of time between a time necessary to etch through layer 120 and to gate 108 and a time to etch through layer 120 and to region 115 or 117, but instead teaches etching completely through layer 120 and to layer 119 both over the gate and over regions 115 and 117 (see col. 9, lines 59-65, which teach etching at least through layer 120 and to layer 119 over the gate and over the drain region). Hence, for at least the reason that the cited reference does not disclose the above noted limitations of claim 1, Applicant respectfully requests the Patent Office withdraw the rejection of claim 1 above.

II. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 2-10 under 35 U.S.C. § 103(a) as being unpatentable over Lee, as applied above, and further in view of U.S. Patent No. 6,0339,622 to Jeng, et al. ("Jeng"). To render a claim obvious, all limitations of

that claim must be taught or suggested by at least one properly combined reference.

Applicant respectfully disagrees with the rejection above and submits that claims 2-7 are patentable over the cited references as they depend from allowable base claim 1, and amended claim 1 is allowable over the cited references.

Specifically, the cited references do not teach or suggest a dielectric layer having a first thickness over a gate and a second different thickness over a junction region, and forming a contact opening through the dielectric layer to the gate comprising etching for a period of time between a time necessary to etch through the dielectric layer on the gate region and a time necessary to etch through the dielectric layer and the junction region, as required by amended claim 1.

Lee does not teach the limitations of claim 1 as pointed by Applicant in the section above.

Also, Jeng teaches a method for forming a self-aligned contact (SAC) by etching BPSG layer 10 through mask 11 in a first step to etch to silicon nitride layer 9c and spacer 9b over and on the sides of gate structure 7 (see col. 3, lines 61 through col. 4, line 17). However, Jeng does not teach etching for a period of time between a time necessary to etch through a dielectric layer on the gate region and a time necessary to etch through the dielectric layer on the junction region, but instead teaches over etching to ensure complete removal of layer 10 (see col. 4, lines 48-52). Thus, Jeng teaches against this limitation of claim 1.

Also, Jeng does not teach that layer 9 has a first thickness over the gate and a second different thickness over the junction region. Thus, the Patent Office has not identified and Applicant is unable to find any teaching or suggestion in Jeng that accounts for the above noted limitations of independent claim 1. Hence,

since neither Lee, Jeng, nor the combination teach the above noted limitations of independent claim 1, and claims 2-7 depend upon allowable base claim 1, Applicant respectfully requests the Patent Office withdraw the rejection above for dependent claims 2-7.

In addition, Applicant disagrees with the rejection above and submits that independent claim 8, as amended, is patentable over the cited references for at least the reasons that the cited references do not teach or suggest forming a contact opening through the dielectric layer to a junction region of the transistor device using a first mask, and forming a contact opening through the dielectric layer to a gate of the transistor device in the active region using a different second mask, as required by claim 8.

As noted by the Patent Office, Lee fails to teach or suggest the limitation noted above.

Next, Jeng teaches a two step process using photo resist shape 11 in the first step to form opening 12b, then removing photo resist mask 11, and selectively removing layer 9c exposed in SAC opening 12b with a chemistry that removes silicon nitride at a rate of about 5 to 20 times faster than the removal rate of layer 10 (the layer having opening 12b therein). However, the Patent Office has not identified and Applicant is unable to find any teaching or suggestion in Jeng using a first mask to form a contact opening to a junction region, and a different second mask to form a contact opening to a gate. Hence, for at least the reason that neither Lee, Jeng, nor the combination, teaches the above noted limitations of amended claim 8, Applicant respectfully requests the Patent Office withdraw the rejection above for that claim.

Moreover, Applicant asserts that the combination of Jeng and Lee

proposed by the Patent Office is improper. For example, using silicon nitride layer 6 above and 9b as a spacer on the side of gate structure 7, thus allowing a SAC structure to be formed through openings in mask 11 to source/drain region 8 (see col. 3, line 61 through col. 4, line 58). However, using the mask as taught by Jeng in the process of Lee would render Lee unsatisfactory for its primary purpose of forming separate contacts to the gate and junction regions.

Specifically, Lee teaches etching to the gate region first and then subsequently etching to the source drain region (see Lee, col. 9, line 48 through col. 10, line 3). Thus using mask 11 of Jeng as a mask to etch through layer 119 of Lee to a source drain region as taught by Jeng (see Jeng, col. 4, line 35 through line 43) would etch away the portion of insulator 130 and 120 between the gate and junction region to create an opening that connects the prior formed opening to the gate of Lee with the subsequent to be formed opening to the source drain of Lee. In other words, the SAC contact opening formed using mask 11 Jeng would allow a contact formed in such an opening to short circuit the opening formed through layer 119 and to the source drain regions of Lee (see Lee, contact 132c) with the contact formed to the gate region (see Lee, contact 132b). As such, the combination of Lee and Jeng proposed by the Patent Office is improper. Hence, for at least this second reason, Applicant respectfully requests the Patent Office withdraw the rejection above of independent claim 8.

Since the cited references do not teach the above noted limitations of claim 8, Applicant asserts that claims 9-10 being dependent upon allowable base claim 8 are also allowable. Hence, Applicant respectfully requests the Patent Office withdraw the rejection above for those dependent claims.

III. Double Patenting

The Patent Office rejections claims 1-10 under the judicially created Doctrine of Obvious Type Double Patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,686,247. In response, the Applicant files the attached Terminal Disclaimer.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Angelo J. Gaz, Reg. No. 45,907

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on May 18, 2005.


Lilian E. Rodriguez

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